## **QUESTION BANK**

SUBJECT : EC8453 - LINEAR INTEGRATED CIRCUITS

SEMESTER/YEAR: IV /II

## Unit I - BASICS OF OPERATIONAL AMPLIFIERS

Current mirror and current sources, Current sources as active loads, Voltage sources, Voltage References, BJT Differential amplifier with active loads, Basic information about op-amps – Ideal Operational Amplifier - General operational amplifier stages - and internal circuit diagrams of IC 741, DC and AC performance characteristics, slew rate, Open and closed loop configurations – JFET Operational Amplifiers – LF155 and TL082.

	PART – A					
Q.No	Questions	BT Level	Competence			
1.	Mention the importance of offset voltage of an operational amplifier?	BTL 1	Remembering			
2.	Define CMRR.	BTL 1	Remembering			
3.	Outline the importance of current mirror circuit used in differential amplifier stages.	BTL 2	Understanding			
4.	Specify the ideal characteristics of Op-amp and methods can be used to produce voltage sources.	BTL 1	Remembering			
5.	How will you understanding the term 'thermal drift' ?	BTL 1	Remembering			
6.	Explain about current mirror with magnification.	BTL 1	Remembering			
7.	Define slew rate and what causes the slew rate?	BTL 1	Remembering			
8.	State loading effect? How can you reduce it?	BTL 2	Understanding			
9.	Why do we use R <sub>comp</sub> resistor?	BTL 2	Understanding			
10.	What is the gain cross over and phase cross over frequencies?	BTL 2	Understanding			
11.	Categorize the characteristics of Non-ideal op-amp.	BTL 3	Applying			
12.	Develop the internal block diagram of an Op-amp.	BTL 3	Applying			
13.	Illustrate the pin diagram of IC 741.	BTL 3	Applying			
14.	Examine the importance of input off set current.	BTL 4	Analyzing			
15.	Analyze about input bias current.	BTL 4	Analyzing			

16.	Inspect the draw backs of using large R <sub>C</sub> in differential amplifier.		BTL 4	Analyzing
17.	Brief the necessity of active loads preferred than passive loads in the input sta an operational amplifier.	ge of	BTL 5	Evaluating
18.	Justify that, why IC741 op-amp not used for high frequency applications?		BTL 5	Evaluating
19.	Calculate the maximum distorted amplitude that a sine wave input of 10 kHz, produce at the output of an op-amp whose slew-rate is 0.5v/µsec.	can	BTL 6	Creating
20.	A Differential amplifier has a differential voltage gain of 2000 and common ngain of 0.2. Determine CMRR.	node	BTL 6	Creating
	PART – B			
1.	Define and explain slew rate. Derive its equation. Also explain method adapted to improving slew rate.	(13)	BTL 1	Remembering
2.	(i) Write down the characteristics and their respective values of an ideal operational amplifier.	(6)	BTL 1	Remembering
3.	<ul><li>(ii) Draw the circuit of basic current mirror and explain its operation.</li><li>(i) Describe about output offset voltage. Explain methods to nullify offset voltage.</li></ul>	(7)	DTI 1	D
	(ii) With neat circuit diagram, explain the operation of voltage reference circuit using temperature compensation.	(6)	BTL 1	Remembering
4.	<ul><li>(i) Discuss on current mirror with magnification.</li><li>(ii) Use appropriate block diagram, explain the general stages of an Op-Amp IC.</li></ul>	(6) (7)	BTL 2	Understanding
5.	<ul> <li>(i) What is input and output voltage and current offset? How are they compensated?</li> <li>(ii) With a neat diagram derive the AC performance close loop Characteristics of Op-amp to discuss on the circuit Bandwidth, Frequency response and slew rate.</li> </ul>	(7) (6)	BTL 2	Understanding
6.	<ul><li>(i) Draw the circuit of basic current mirror and explain its operation.</li><li>(ii) Give the detail of the DC analysis of a basic differential amplifier with necessary diagram.</li></ul>	(6) (7)	BTL 3	Applying
7.	Obtain the expression for differential gain, common mode gain, CMRR, $R_{\rm I}$ and $R_{\rm O}$ of an emitter coupled differential amplifier.	(13)	BTL 4	Analyzing
8.	<ul> <li>(i) Sketch the Wilson current source and write short note about it.</li> <li>(ii) Using suitable diagram and necessary equations, explain the concept of Widlar current source used in op-amp circuit.</li> </ul>	(5) (8)	BTL 3	Applying  Analyzing
9.	Show the transfer characteristics of dual input differential amplifier showing the linear and limiting regions. Comment on the same.	(13)	BTL 4	Understanding
10.	(i) Derive the functional parameters for an inverting mode negative feedback gain circuit with a 741op-amp in IC inverting mode, with R1=1Kohm, Rf=40Kohm and compute Af, Rif, Rof, BW, offset voltage.	(7)	BTL 4	Analyzing
	(ii) Discuss briefly on the differential mode Instrumentation amplifier.	(6)	BTL 3	Applying
11.	Examine the working principle of BJT differential amplifier with active load.	(13)	BTL 5	Evaluating

12.	<ul><li>(i) Compose the concept of Widlar current source used in op-amp circuit With suitable circuit diagram and necessary equations.</li><li>(ii) Justify the preference of active load over passive load.</li></ul>	(10)	BTL 6	Creating	
13.	Write note on LF155 JFET input operational amplifier and TL082 wide bandwidth dual JFET input operational amplifier with necessary diagram.	(13)	BTL 1	Remembering	
14.	State and explain about CMRR, $A_{\text{d}}$ , $A_{\text{c}}$ and suggest a method to improve CMRR.	(13)	BTL 4	Analyzing	
	PART – C		I		
1.	Derive the transfer characteristics of dual input differential amplifier showing the linear and limiting regions. Comment on the same.	(15)	BTL 5	5 Evaluating	
2.	<ul> <li>(i) A square wave peak-to-peak amplitude of 50mV has to be amplified to a peak-to-peak amplitude of 3V, with rise time of 4 μs or less. Can IC741 be used?</li> <li>(ii) A IC741 Op-Amp whose slew rate is 0.5V/μs is used as an inverting amplifier with a gain of 50.The voltage gain Vs frequency curve of IC741 is flat up to 20 kHz. What maximum peak to peak input signal can be applied without distorting the output?</li> </ul>	(5) (10)	BTL 6	6 Creating	
3.	Explain in detail the A.C analysis of dual input, balanced output differential amplifier or derive the expression for differential gain, common mode gain, CMRR, $R_I$ and $R_O$ of an emitter coupled differential amplifier.	(15)	BTL 5	5 Evaluating	
4.	<ul> <li>(i) Assuming slew rate for 741 is 0.5 V/μs, what is the maximum undistorted sine wave that can be obtained for</li> <li>(a) 12 V Peak to Peak.</li> <li>(b) 2 V Peak to Peak.</li> <li>(ii) An inverting amplifier using the 741C must have a flat response up to 40 kHz. The gain of the amplifier is 10. What maximum peak-to-peak input signal can be applied without distortion the output</li> </ul>	(8)	BTL 6	6 Creating	

# UNIT II APPLICATIONS OF OPERATIONAL AMPLIFIERS

Sign Changer, Scale Changer, Phase Shift Circuits, Voltage Follower, V-to-I and I-to-V converters, adder, subtractor, Instrumentation amplifier, Integrator, Differentiator, Logarithmic amplifier, Antilogarithmic amplifier, Comparators, Schmitt trigger, Precision rectifier, peak detector, clipper and clamper, Low-pass, high-pass and band-pass Butterworth filters.

PARI – A					
Q.No	Questions	BT Level	Competence		
1.	Mention the advantages of variable trans conductance technique?	BTL 2	Understanding		
2.	Summarize the other name for Clipper circuit?	BTL 2	Understanding		
3.	What is the need for converting a first order filter into a second order filter?	BTL 2	Understanding		
4.	How is the current characteristic of a PN junction employed in a log amplifier?	BTL 1	Remembering		
5.	Compare the performance of inverting and non-inverting operational amplifier configurations.	BTL 4	Analyzing		
6.	Give the applications of inverting & non- inverting amplifiers.	BTL 1	Remembering		
7.	Draw the inverting & non- inverting amplifiers with appropriate equations.	BTL 3	Applying		
8.	List the applications for each of the following circuits: Voltage follower, Peak detector, Schmitt trigger, Clamper.	BTL 2	Understanding		
9.	Why integrators are preferred over differentiators in analog computers?	BTL 5	Evaluating		

10.	Summarize the frequency expressions for LPF, HPF and BPF.		BTL 1	Remembering
11.	Enumerate the advantages & disadvantages of passive filters?		BTL 1	Remembering
12.	Sketch the opamp integrator & differentiator circuit with necessary equation	n.	BTL 3	Applying
13.	Define comparator and function of a phase shift circuit?		BTL 1	Remembering
14.	Give some important features of an instrumentation amplifier.		BTL 1	Remembering
15.	Construct an adder circuit using op-amp to get the output expression as Vo $(0.1V1 + V2 + 5V3)$	= -	BTL 3	Applying
16.	Demonstrate the need for frequency compensation in practical op-amps		BTL 4	Analyzing
17.	Show the necessity of active guard drive in an instrumentation amplifier.		BTL 4	Analyzing
18.	Find the output voltage of the following circuit. Given R1 =R2 = $10k\Omega$ and $100$	Rf=	BTL 6	Creating
19.	How does precision rectifier differ from the conventional rectifier?		BTL 5	Evaluating
20.	Design an amplifier with a gain of -10 and input resistance equal to $10 \text{ k}\Omega$ .		BTL 6	Creating
20.	PART – B		DILU	Creating
1.	<ul> <li>(i). With a suitable circuit diagram, explain the operating principle of an instrumentation amplifier and derive its gain.</li> <li>(ii). Design a second order Butterworth low-pass filter having upper cut-off frequency of 2.1961 kHz</li> </ul>	(7) (6)	BTL 2	Understanding
2.	Compare and contrast Adder, Subtractor, and Averaging circuit using opamp with equations.	(13)	BTL 4	Analyzing
3.	Write the operation of current to voltage and Voltage to current converter circuits.	(13)	BTL 1	Remembering
4.	(i) Draw and explain the operation of Triangular wave generator.	(5)	BTL 1	Remembering
	(ii) Write short notes on second order Low Pass Butterworth filter (Sallen-key filter).	(8)	BTL 1	Remembering
5.	Derive the expression for log computation using op-amp and explain	(13)	D	T 1
	necessary circuit diagram.		BTL 5	Evaluating
6.	With neat figures describe the circuit using op-amps on the following of (i). Integrator and double integrator circuit.  (ii). First order High pass filter	(7) (6)	BTL 1	Remembering
7.	Draw and explain the circuit of a voltage to current converter if the load is i) Floating (7) ii) Grounded (6)		BTL 1	Remembering
8.	<ul> <li>(i) Design an OP-AMP based first order active low pass filter.</li> <li>(ii) Create if a bandpass filter has a lower cut-off frequency f<sub>L</sub>=250Hz and a higher cut-off frequency f<sub>H</sub>= 2500Hz the find its bandwidth and the resonant frequency.</li> </ul>	(7) (6)	BTL 6	Creating
9.	<ul><li>i) Analyze the distinct features of the precision diode.</li><li>ii) Using appropriate equations discuss about the working of Half wave Precision Rectifier.</li></ul>	(3) (10)	BTL 4 BTL3	Analyzing Applying
10.	<ul><li>(i). With neat sketch explain the working of Full wave Precision Rectifier in detail.</li><li>(ii). Sketch the Integrator circuit and explain the working principle in</li></ul>	(8) (5)	BTL 3	Applying

	detail.			
11.	<ul><li>i) Explain With neat diagram and operation of Schmitt trigger.</li><li>ii) Summarize a detailed note about op-amp band pass filter.</li></ul>	(5) (8)	BTL 2	Understanding
12.	Conclude that how antilog computations are performed using IC-741 explain using circuits and necessary equations.	(13)	BTL 5	Evaluating
13.	(i). Examine the principal of operation of Voltage follower with the neat	(6)	BTL 4	Analyzing
	circuit diagram and mathematical expressions.  (ii). With the neat circuit diagram and mathematical expressions, explain the operation of Scale changer.	(7)	BTL 3	Applying
14.	Discuss wave shaping circuits using operational amplifier.	(13)	BTL 2	Understanding
	PART – C			
1.	Evaluate Inverting adder and Non-inverting adder with neat circuit diagram mathematical expressions.	n and (15)	BTL 5	Evaluating
2.	Design a differentiator using Op-Amp to differentiate an input signal with 200 Hz and also draw the output waveforms for a sine-wave and square-wainput of 1V peak at 200 Hz.		BTL 6	Creating
3.	Given a bandpass filter with resonant frequency f <sub>r</sub> of 1000Hz and a bandw (BW) of 3000Hz, find its.  (a). Quality factor.  (b). Lower Cut-off frequency.  (c). High Cut-off Frequency	idth	BTL 6	Creating
4.	Using Op-amps circuit examine the operation of.  (i) Zero cross Detector, Clipper and Clamper circuit	(8) (7)	BTL 5	Evaluating

## UNIT III ANALOG MULTIPLIER AND PLL

Analog Multiplier using Emitter Coupled Transistor Pair Gilbert Multiplier cell – Variable transconductance technique, analog multiplier ICs and their applications, Operation of the basic PLL, Closed loop analysis, Voltage controlled oscillator, Monolithic PLL IC 565, application of PLL for AM detection, FM detection, FSK modulation and demodulation and Frequency synthesizing, Clock synchronization

PART A				
Q.No	Questions	BT Level	Competence	
1.	Outline the basic building blocks of PLL.	BTL 1	Remembering	
2.	Define capture range and lock range of PLL.	BTL 1	Remembering	
3.	What is Pull- in time?	BTL 1	Remembering	
4.	For perfect lock, what should be the phase relation between the incoming signal and VCO output signal?	BTL 4	Analyzing	
5.	Mention the classification of phase detector. Write about switch type phase detector.	BTL 2	Understanding	

6.	Illustrate the problems associated with switch type phase detector	BTL 2	Understanding
7.	Why VCO is also called as V to F converter?	BTL 1	Remembering
8.	On what parameters does the free running frequency of VCO depend on?	BTL 3	Applying
9.	Give the expression for the VCO free running frequency.	BTL 2	Understanding
10.	Demonstrate Voltage to Frequency conversion factor.	BTL 2	Understanding
11.	Describe the purpose of having a low pass filter in PLL.	BTL 3	Applying
12.	Discuss the effect of having large capture range.	BTL 6	Creating
13.	Estimate that the frequency stability obtained in a PLL by use of VCO.	BTL 5	Evaluating
14.	How are square root and square of a signal obtained with multiplier circuit?	BTL 1	Remembering
15.	Identify the merits of companding	BTL 3	Applying
16.	List out the applications of OTA.	BTL 1	Remembering
17.	Asses the need of pre-distortion circuits in Gilbert analog multiplier and how is the configuration of Gilbert multiplier done with pre-distortion circuits.	BTL 5	Evaluating
18.	Analyze the necessity of modulation.	BTL 4	Analyzing
19.	Develop the circuit of AM detector using PLL.	BTL 6	Creating
20.	Distinguish the advantages & disadvantages of monolithic PLLs over	BTL 4	Analyzing
	Discrete PLLs.  PART – B		
1.	PART – B  How would you describe the block diagram of PLL and derive the expression	BTL 1	Remembering
	PART – B	BTL 1 BTL 2	Remembering Understanding
1.	PART – B  How would you describe the block diagram of PLL and derive the expression for Lock range and capture range. (13)  Illustrate the operation of VCO with neat block diagram. Also derive an		<u> </u>
1.	PART – B  How would you describe the block diagram of PLL and derive the expression for Lock range and capture range. (13)  Illustrate the operation of VCO with neat block diagram. Also derive an expression for f <sub>0</sub> . (13)  (i) Analyze the Gilbert's four quadrant multiplier cell with a neat circuit diagram. (8)	BTL 2	Understanding  Analyzing
1. 2. 3.	How would you describe the block diagram of PLL and derive the expression for Lock range and capture range. (13)  Illustrate the operation of VCO with neat block diagram. Also derive an expression for f <sub>0</sub> . (13)  (i) Analyze the Gilbert's four quadrant multiplier cell with a neat circuit diagram. (8)  (ii) Identify how a frequency doubler can be realized using this cell. (5)	BTL 2 BTL 4 BTL 3	Understanding  Analyzing Applying
1. 2. 3.	How would you describe the block diagram of PLL and derive the expression for Lock range and capture range. (13)  Illustrate the operation of VCO with neat block diagram. Also derive an expression for f <sub>0</sub> . (13)  (i) Analyze the Gilbert's four quadrant multiplier cell with a neat circuit diagram. (8)  (ii) Identify how a frequency doubler can be realized using this cell. (5)  Discuss any three applications of PLL in detail. (13)  Explain the purpose and functioning of  (i) Frequency division circuit using PLL IC565 (7)  (ii) Frequency synthesizer (6)	BTL 2 BTL 4 BTL 3	Understanding  Analyzing Applying  Creating
1. 2. 3. 4. 5.	How would you describe the block diagram of PLL and derive the expression for Lock range and capture range. (13)  Illustrate the operation of VCO with neat block diagram. Also derive an expression for f <sub>0</sub> . (13)  (i) Analyze the Gilbert's four quadrant multiplier cell with a neat circuit diagram. (8)  (ii) Identify how a frequency doubler can be realized using this cell. (5)  Discuss any three applications of PLL in detail. (13)  Explain the purpose and functioning of  (i) Frequency division circuit using PLL IC565 (7)  (ii) Frequency synthesizer (6)	BTL 2  BTL 4  BTL 3  BTL 6  BTL 2	Understanding  Analyzing Applying  Creating  Understanding
1. 2. 3. 4. 5.	How would you describe the block diagram of PLL and derive the expression for Lock range and capture range. (13)  Illustrate the operation of VCO with neat block diagram. Also derive an expression for f <sub>0</sub> . (13)  (i) Analyze the Gilbert's four quadrant multiplier cell with a neat circuit diagram. (8)  (ii) Identify how a frequency doubler can be realized using this cell. (5)  Discuss any three applications of PLL in detail. (13)  Explain the purpose and functioning of (i) Frequency division circuit using PLL IC565 (7)  (ii) Frequency synthesizer (6)  (i) Estimate the working principle of operational Transconductance Amplifier (OTA). (8)  (ii) Explain the application of VCO for FM generation. (5)  (i) Define capture range and lock range. (3)  (ii) Explain the process of capturing the lock and also derive for capture	BTL 2  BTL 4 BTL 3  BTL 6  BTL 2	Understanding  Analyzing Applying  Creating  Understanding  Applying

10.	(i) Examine the multiplier cell using emitter- coupled transistor pair. (8) (ii) Analyze that the output voltage is proportional to the product of the two input voltages and state their limitations. (5)	BTL 4	Analyzing
11.	Briefly explain the use of PLL for FM detection and the process of FSK demodulation. (13)	BTL 1	Remembering
12.	Discuss the following applications of Analog Multiplier ICs (i) Voltage squarer (ii) voltage divider (iii) square rooter (iv) Phase angle detector (3) (3)	BTL 2	Understanding
13.	Measure the closed loop analysis of PLL with necessary diagrams. (13)	BTL 4	Analyzing
14.	Explain the operation of a variable trans conductance multiplier circuit.  Derive the expression for its output voltage. (13)	BTL 4	Analyzing
	PART - C		
1.	<ul> <li>(i). Discuss the basic analog multiplication techniques.</li> <li>(ii). Develop the expression for free running frequency of voltage controlled oscillator.</li> </ul>	BTL 6	Creating
2.	(i). Determine the output frequency $f_0$ , lock range $\Delta f_L$ and capture range $\Delta f_C$ of IC 565. Assume $R_1$ =15K $C_1$ =0.01 $\mu$ F, C=1 $\mu$ F and the supply voltage is +12V. (9) (ii). A PLL IC connected as an FM demodulator $R_1$ = 10K $\Omega$ $C_1$ =0.04 $\mu$ F. The supply voltage is +12 V. Determine (a) free-running frequency. (b) Lock-range and (c). Capture range. (6)	BTL 5	Evaluating
3.	<ul> <li>(i). For PLL 565, given the free-running frequency as 100KHz, the demodulation capacitor of 2μf and supply voltage is ±6V, determine the lock and capture frequencies and identify the component values.</li> <li>(ii) Determine the change in dc controlled voltage v<sub>c</sub> during lock, if input signal frequency f<sub>s</sub> = 20kHz, the free running frequency is 21 kHz and the V/F transfer coefficient of VOC is 4kHz/V.</li> </ul>	BTL 5	Evaluating
4.	Construct the block diagram and explain principle of working, characteristics and applications of:  (i) Frequency synthesizer.  (ii) Frequency shift keying (FSK) Demodulator  (7)	BTL 6	Creating

#### UNIT IV ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS

Analog and Digital Data Conversions, D/A converter – specifications weighted resistor type, R- 2R Ladder type, Voltage Mode and Current- Mode R - 2R Ladder types - switches for D/A converters, high speed sample- and- hold circuits, A/D Converters – specifications - Flash type - Successive Approximation type - Single Slope type – Dual Slope type - A/D Converter using Voltage- to- Time Conversion - Over- sampling A/D Converters, Sigma- Delta converters

## PART A

Q. No	Questions	BT Lev		Con	npetence	
1.	Classify the A/D converters based on their operational features.	BTL	. 2	Und	erstanding	
2.	List the direct type ADCs.	BTL	, 4	Ana	Analyzing	
3.	What is the function of integrating type converter? List out some integrating type converters.	BTL	. 1	Ren	nembering	
4.	Review the principle of operation of successive Approximation ADC.	BTL	. 2	Und	erstanding	
5.	Mention the main advantages of integrating type ADCs.	BTL	. 1	Ren	nembering	
6.	Define Sampling .	BTL	. 1	Ren	nembering	
7.	Compare the advantages and drawbacks of a dual- slop ADC.	BTL	. 2	Und	erstanding	
8.	Distinguish between conversion time and settling time.	BTL	, 4	Ana	lyzing	
9.	Find the number of resistors required for an 8-bit weighted resistor D/A converter. Consider the smallest resistance is R and obtain those resistance values.	BTL	, 5	Eva	luating	
10.	Give the advantages of inverted R-2R (current type) ladder D?A converter over R -2R(voltage type) D/A converter?	BTL	. 1	Ren	nembering	
11.	Brief the need for electronic switches in D/A converter and mention the names of the switches used in MOS transistors.	BTL	. 1	Ren	nembering	
12.	Summarize delta modulation.	BTL	TL 2 U		Understanding	
13.	How would you justify which type of ADC is the fastest?	BTL	L 5 Eva		Evaluating	
14.	Outline the principle of operation of voltage to time conversion.		STL 1 R		Remembering	
15.	Calculate the values of LSB and MSB for an 8- bit DAC for 0V to 10V range.	BTL	TL 6 Cı		Creating	
16.	Interpret the features of granular error and slope overload error.	BTL	. 3	Applying		
17.	An 8 bit A/D converter accepts an input voltage signal of range 0 to 12v. What is the digital output for an input voltage of 6V?	BTL	. 3	Applying		
18.	Evaluate the number of comparators required for realizing a 4-bit flash ADC.	BTL	6	Crea	ating	
19.	Compare and contrast binary weighted and R- 2R ladder DAC.	BTL	, 4	Ana	lyzing	
20.	Identify the need of Sample and hold circuit and Why schottky diodes are used in sample and hold circuits?	BTL	. 3	App	lying	
	PART – B					
1.	<ul> <li>(i) How would you categorize A/D converters?</li> <li>(ii) Discuss the working principle of successive approximation type ADC.</li> </ul>	(6) (7)	ВТ	TL 2	Understanding	
2.	<ul> <li>(i) Estimate the working of R- 2R ladder type DAC.</li> <li>(ii) Compare binary weighted DAC with R- 2R ladder network DAC.</li> </ul>	(7) (6)		TL 4	Analyzing	
3.	<ul><li>(i) With circuit schematic explain analog switches using FET.</li><li>(ii) What is meant by resolution, offset error in ADC.</li></ul>	(7) (6)	ВТ	L 1	Remembering	
4.	<ul> <li>(i) Explain in detail on the operational features of 4-bit weighted resistor type D/A converter.</li> <li>(ii) Differentiate between current mode and voltage mode R-2R ladder D/A converters.</li> </ul>	(7) (6)	ВТ	TL 4	Analyzing	

5.	Dese Exp	cribe the operation of any two direct type of ADCs and	(13)	BTL 1	Remembering
6.	Sun	nmarize the following Digital to Analog & Analog to Digital version techniques.		BTL 2	Understanding
		Flash type ADC.	(7)		
		Weighted resistor DAC.	(6)		
7.	(i)	Draw the diagram of sample and hold circuit.	(6)	BTL 1	Remembering
•	(ii)	State how you will reduce its hold mode droop.	(7)		
8.		ign a 4-bit binary weighted resistor DAC for the following effications: Use LM741 op- amp, $R = 10k\Omega$ , $V_{ref} = 2.5V$ and	(13)	D/DI 4	A 1 .
		scale output = $5V$ .		BTL 4	Analyzing
9.	A d	ual slope ADC has a full scale input of 2 Volts .It uses an	(13)		
		grating time of 10ms and integrating capacitor of 0.1µf.the		BTL 3	Applying
		imum magnitude of the integrator output should not exceed		DILS	Applying
		Calculate the value of the integrating resistor.			
10.	Des sket	scribe in detail about the single slope type ADC with neat ch.	(13)	BTL 3	Applying
11.	(i)	Sketch the block diagram and explain the working of Charge	(6)		
114		Balancing VFCS	(0)		
	(ii)	With functional block diagram explain A/D converter using	(7)	BTL 1	Remembering
		Voltage to Time converter with input and output			
12.	(i)	waveforms.  Elaborate the operation of high speed sample and hold	(9)		
14.	(ii)	circuits.	(9)		
		Develop a system employs a 16-bit word for representing		BTL 6	Creating
		the input signal. If the maximum output voltage is set 2V,	(4)		C
		calculate the resolution of the system and its dynamic range.			
13.	(i)	Illustrate the various important specifications of both D/A	(7)	BTL 2	Understanding
		and A/D converters generally specified by the manufactures			
	(ii)	are analysed.  A 8-bit A/D converter accepts an input voltage signal of	(6)		
		range 0 to 9V, What is the minimum value of the input	(0)		
		voltage required for generating a change of 1 least			
		significant bit ? specify the digital output for an input			
		voltage of 4 V. What input voltage will generate all 1s at the			
1.4	(;)	A/D converter output?	(2)	DTI 5	Essalas Aires
14.	(i)	The basic step of a 9-bit DAC is 10.3mV. If 000000000 represents 0V, what output is produced if the input is	(3)	BTL 5	Evaluating
		101101111?			
	(ii)	Calculate the values of the LSB, MSB and full scale output	(5)		
	(;;;	for an 8-bit DAC for the 0 to 10V range.			
	(iii	What output voltage would be produced by a D/A converter	/=:		
	′	whose output range is 0 to 10V and whose input binary	(5)		
		number is (i) 10 (for a 2-bit D/A converter)			
		(ii) 0110 (for a 4-bit DAC)			
		(iii) 10111100 (for a 8-bit DAC)			
	1	PART - C		1	l

1.	(i)	For a 4-bit R-2R ladder D/A converter assume that the full	(10)	BTL6	Creating
		scale voltage is 16V.Calculate the step change in output			
	(::)	voltage on input varying from 01111 to 1111.	(5)		
	(ii)	Discuss the important specification of Data Converters.	(5)	DEL 6	T 1
2.	(i)	Compare single slope ADC and dual slope ADC.	(3)	BTL 5	Evaluating
	(ii)	Draw the circuit and explain the working of dual slope A/D	(7)		
	<b>,</b>	converter.	(7)		
	(iii	Calculate t <sub>2</sub> for a particular dual slope ADC, t <sub>1</sub> is 83.33ms	( <b>=</b> )		
	)	and the reference voltage is 100mv if	(5)		
		1. V <sub>1</sub> is 100 mv and			
		2. 200 mv			
3.		gn the R-2R 4-bit converter and assume that feedback	(15)		
		tance $R_f$ of the op-amp is variable, the resistance $R=10k\Omega$			
		$V_R = 10V$ . Determine the value of $R_f$ that should be connected			
	to ac	chieve the following output conditions.		BTL 6	Creating
	(	The value of 1 LSB at the output is 0.5V		DIL 0	Crouting
	(	ii) An analog output of 6V for a binary input of 1000.			
		iii) The Full-scale output voltage of 12V			
	(	iv) The actual maximum output voltage of 10V			
4.	(i)	Derive the Inverted or Current mode R-2R Ladder Digital to	(10)	BTL 5	Evaluating
		analog converter and explain.			
	(ii)	Examine the inverted R-2R ladder (refer above question)			
		has R=Rf=10k $\Omega$ and V <sub>R</sub> =10V. Calculate the total current	(5)		
		delivered to the op-amp and the output voltage when the			
		binary input is 1110.			

## UNIT V WAVEFORM GENERATORS AND SPECIAL FUNCTION ICS

Sine-wave generators, Multivibrators and Triangular wave generator, Saw-tooth wave generator, ICL8038 function generator, Timer IC 555, IC Voltage regulators – Three terminal fixed and adjustable voltage regulators - IC 723 general purpose regulator - Monolithic switching regulator, Low Drop – out(LDO) Regulators -Switched capacitor filter IC MF10, Frequency to Voltage and Voltage to Frequency converters, Audio Power amplifier, Video Amplifier, Isolation Amplifier, Opto-couplers and fibre optic IC.

PART A						
Q. No	Questions	BT	Competence			
		Level				
1.	What is the need for voltage regulator ICs?	BTL 2	Understanding			
2.	List the characteristics and applications of Opto coupler.	BTL 4	Analyzing			
3.	Sketch a fixed voltage regulator circuit and state its operation.	BTL 1	Remembering			
4.	Mention the conditions for oscillation.	BTL 2	Understanding			
5.	What is a switching regulator?	BTL 1	Remembering			
6.	List the applications of 555 timer in Monostable mode of operation.	BTL 1	Remembering			
7.	Classify the three different wave forms generated by ICL8038.	BTL 2	Understanding			
8.	Mention the need for current limiting in voltage regulators.	BTL 4	Analyzing			
9.	Compare Linear regulator and Switched mode regulator.	BTL 5	Evaluating			

10.				BTL 1	Remembering
11	monolithic IC voltage regulators.			BTL 1	Damamhanina
11.		Draw the functional block diagram of IC 723 regulator.			Remembering
12.	Compare the principle of linear regulator and a switched mode power supply.				Understanding
13.	How would you classify an opto-coupler , also mention the current transfer			BTL 5	Evaluating
		of an opto coupler.			
14.		ne line and load regulation of a regulator.		BTL 1	Remembering
15.	In a Astable multivibrator of 555 times $R_A$ =606k $\Omega$ and C=0.1 $\mu$ F. Calculate (a) t <sub>HIGH</sub> (b)t <sub>LOW</sub> (c) free running frequency (d) duty cycle (D).			BTL 6	Creating
16.	How does switched capacitor emulate resistor?			BTL 3	Applying
17.		With reference to a VCO, define voltage to frequency conversion factor $K_v$ .		BTL 3	Applying
18.	In a monostable multivibrator using 555 timer, $R=100k\Omega$ and the time delay			BTL 6	Creating
		00ms.Find the value of C.	J		
19.	List	List the types of Multivibrator.			Analyzing
20.		Give reasons for the purpose of connecting a capacitor at the input and		BTL 3	Applying
	outp	ut side of an IC voltage regulator?			
	1	PART – B	ı		
1.		Write a short notes on	(5)	DTI A	TTo decode a disc
		<ul><li>(i) Opto couplers.</li><li>(ii) Switched capacitor filter</li></ul>	(5) (4)	BTL 2	Understanding
		(iii)Audio power amplifier	(4)		
		(m)/ tudio power ampirier	(4)		
2.	(i)	Demonstrate and explain the functional diagram of LM 380	(8)	BTL 2	Understanding
		power amplifier.	(5)		
	(ii)	Illustrate the essential characteristics of power amplifier.			
3.	(i)	What is 555 timer? Explain the working of 555 timer as	(7)	BTL 1	Remembering
		Monostable Multivibrator.			
		Derive an expression for the frequency of oscillation with			
	(ii)	relevant waveforms.	(6)		
4.	(i)	Analyze and explain the operation of switching regulator with	(8)	BTL 4	Analyzing
		neat diagram.			
	(ii)	Examine the operation of frequency to voltage converters.	(5)		
5.	(i)	Show the working of Astable Multivibrator using op-amp.	(8)	BTL 1	Remembering
	(ii)	Outline any one application of Astable Multivibrator in detail.	(5)		
6.	(i)	Design a phase shift oscillator to oscillate at 100 Hz.	(6)	BTL 6	Creating
	(ii)	Design a frequency to voltage converter using IC VFC 32 for	(7)		
		a full scale output of 8V for a full scale input frequency of 80kHz with a maximum ripple of 8mV.			
7.	(i)	Define voltage regulator and explain the working of Linear	(8)		
	(-)	Voltage regulator with neat circuit diagram using op-amps.		BTL 1	Remembering
	(ii)	List any two important features of linear voltage regulator	(5)		
		IC723.			
8.	(i)	Assess the working principle of monolithic switching	(8)	BTL 5	Evaluating
	(ii)	regulator.	(5)		

	1		1		
		Evaluate how the frequency is computed using voltage to			
0	(*)	frequency converter.	(0)		
9.	(i)	With neat diagram, explain the operation of an astable and	(8)	DEL 0	A 1 '
		monostable multivibrators using opamp.	(5)	BTL 3	Applying
	(ii)	Illustrate the functional diagram and connection diagram of a	(5)		
		low voltage regulator and explain.			
10.	(i)	Develop the basic principle of function generator? Draw the	(7)		
		schematic of ICL 8038 function generator and discuss its		BTL3	Applying
		features.			
	(ii)	Solve the expression for the frequency of a triangular	(6)		
		waveform generator and explain the circuit.			
11.	(i)	Describe the 555 timer IC.design a astable multivibrator circuit	(6)		
		to generate output pulses of 25%,50% duty cycle using a 555		BTL 2	Understanding
		timer IC with the choice of C=0.01µF and a frequency of 4			
	(ii)	kHz.	(7)		
		Demonstrate Monostable multivibrator with necessary			
		diagrams and derive for ON time and recovery time.			
12.	(i)	Interpret the working of monostable multivibrator.	(10)		
	(ii)	What are opto-couplers?	(3)	BTL 1	Remembering
13.	(i)	Analyzing the working of a general purpose voltage regulator.	(10)		
	(ii)	Justify the need for isolation amplifiers.	(3)	BTL 4	Analyzing
4.4	` ′				, &
14.		n a neat circuit diagram, explain the working of linear voltage	(13)	DTI 4	A 1 '
	regu	lator using operational amplifier.		BTL 4	Analyzing
	ı	PART C			
Q. No		Questions		BT	Competence
	(*)	7	(0)	Level	
1.	(i)	In a astable multivibrator using 555 timer Ra=6.8K,Rb = 3.3K,	(8)	DTI 5	Facility of the s
	(;;)	C=0.1uF.Calculate the free running frequency.	(7)	BTL 5	Evaluating
	(ii)	Design a square wave generator using 555timer for a frequency of 120Hz and 60% duty cycle. Assume C=0.2uF.	(7)		
2.	(i)	Analyze the important features and pin details of switched	(8)		
4.	(1)	capacitor filter IC MF10.	(6)	BTL 6	Creating
	(ii)	Design a wave generator using 555 timer for a frequency of	(7)	DILO	Creating
	(11)	110Hz and 80 % duty cycle. Assume C =0.12μF	(')		
3.	Deri	ve the expression and circuit operation for LM 380 Audio power	(15)		
		lifier.		BTL 5	Evaluating
4.		ign an adjustable voltage regulator circuit using LM 317 for the	(15)		<u> </u>
		owing specifications: Input dc voltage =13.5 V; Output dc		BTL 6	Creating
		age = 5 to 9V; Load current (maximum) = 1A.			
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